10. OTHER ACTIVITIES ON CONTROL, DATA ACQUISITION AND SIGNAL PROCESSING

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10.1. INTRODUCTION

This chapter reports the activities carried out in the frame of the following research lines:

- Development of a low-cost, fully integrated, real time control and data acquisition system;
- Development of a DSP-based real-time control system;
- Development of PCI instrumentation for control and data acquisition;
- Variational approach to the extraction of quadrature from broadband reflectometry signals.

10.2. DEVELOPMENT OF A LOW-COST, FULLY-INTEGRATED REAL-TIME CONTROL AND DATA ACQUISITION SYSTEM

Following the development of the VME and CAMAC Fast Timing and Event Management System for the MAST tokamak, CFN has decided to start the development of a low-cost, fully-integrated real-time control and data acquisition system.

The following main activities were performed:

- Beginning of the conceptual study of the system;
- Study of new emerging buses for digital instrumentation;
- Analysis of the commercial DSP-based and FPGA-based systems.

10.3. DEVELOPMENT OF A DSP-BASED REAL-TIME CONTROL SYSTEM

10.3.1. Introduction

The following main activities were made:

- Finalisation of the assembly and testing of the hardware of the VME version of this system;
- Development of the operation software.

10.3.2. High performance real-time control and event detection DSP based VME system

This system is composed by a commercial CPU board (VME HOST) and several on-site made intelligent modules inserted in the same VME crate. It can operate in stand-alone mode or with the Fast Timing and Event Management System developed by CFN/IST. The VME HOST manages and configures all the modules in the VME crate and perform the interface to the main experiment control and database. The intelligent modules perform data acquisition for real-time processing in order to detect events and trigger the timing system of the data acquisition system of the experiment. They can also make real-time control and waveform generation.

The on-site module consists in a 6U, A32/D16 VME bus printed circuit board with 4 independent Acquisition, Processing and Control (APC) channels (Figure 10.1) specially designed for data acquisition, real-time parallel processing and control.

Each APC channel (Figure 10.2) is composed of:

- One analog differential input for data acquisition with 12-bit resolution, +/-5V voltage range, independent software programmable sampling rate of up to 40 MSPS, and a FIFO memory of up to 32 kword;
- One 32-bit floating point DSP (TMS320C44) that can process up to 40MIPS/80 MFLOPS;
- Up to 128 kwords 32-bit wide SRAM for DSP program and data;
- One analog output for control with 14-bit resolution, +/-5V voltage range, independent software programmable update rate of up to 100 MSPS and a FIFO memory of up to 32 kword.

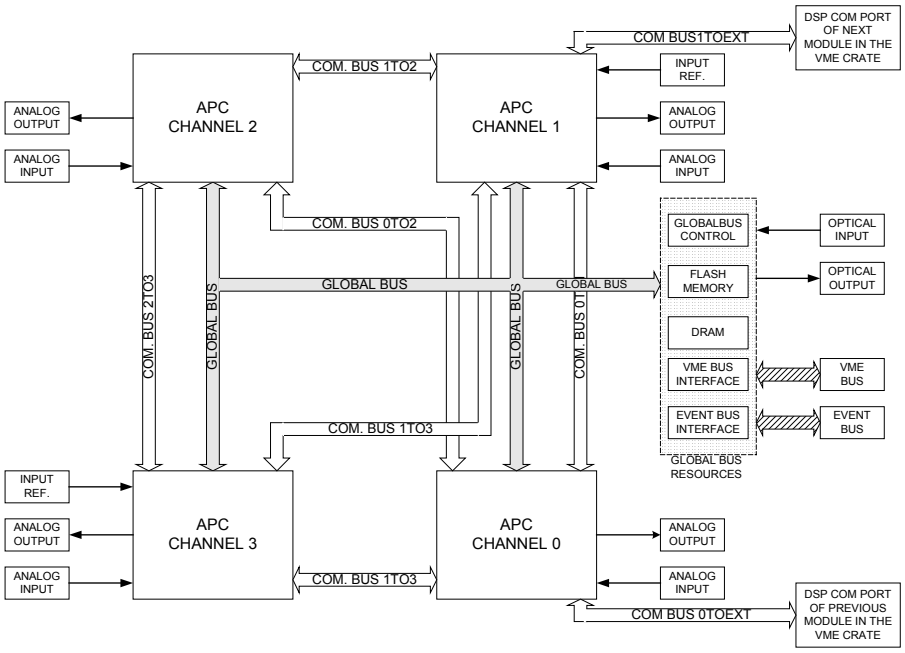

Figure 10.1 – Architecture of the intelligent module

Data acquisition can be performed in four modes of operation: continuous, post-trigger, pre-trigger, and centred trigger.

The DAC circuit has two operating modes: control mode and waveform generator. In this last mode the DAC block can generate, in a stand-alone way (without the intervention of the DSP), periodic signals with up to 32 kwords per period. The DAC circuit can have an external reference input for hardware multiplying if needed.

The DSPs of all APC channels are synchronised and can directly interchange data among each other for parallel processing thus increasing the processing capacity of the module. The module is cascadable, which means that two DSPs in a module can also directly interchange data with two DSPs in two other modules. This enables the direct interconnection of DSPs of up to two times the maximum number of modules in a VME crate.

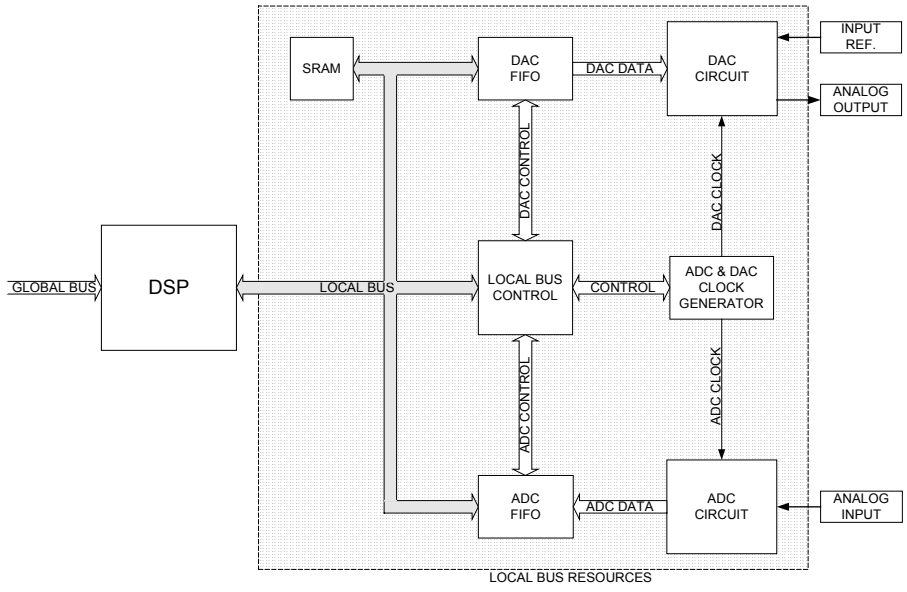

Figure 10.2 – Architecture of each acquisition, processing and control channel

In the module there are also up to 16 Mwords of 16-bit wide DRAM to keep acquired data. This memory is shared with the VME HOST and may be used as a memory buffer between the data acquisition and the VME bus or even to exchange data between DSPs.

In order to have external synchronisation (input trigger) and the ability to trigger other modules (output trigger), the module has a digital input and a digital output, both with optical interface.

One of the most important features of the module is the interface to the Event Bus as a slave (in the VME P2 connector). This bus, designed by CFN/IST, gives the possibility to the module of to send events very fast to the Timing and Event Management System developed by CFN/IST, and this way, generate synchronised triggers to the main data acquisition and control system.

The module can generate interrupts to the VME HOST, if needed, and all the configuration of the board, including the VME bus address, is jumperless.

The control and setup of the module is made by the VME HOST, which sends and receives commands through FIFOs to or from the DSPs.

The digital signal processing algorithms ran by the DSPs, can be downloaded by the VME HOST or can reside in its firmware together with the Operative System. This firmware is kept in a Flash memory with up to 512 kbytes of memory and is shared by all DSPs. The use of a FLASH memory to keep the firmware of the module has two great advantages: i) during power on or reset, the module can start and run an application in a stand alone mode – meaning that it doesn't need the intervention of the VME HOST to download programmes or algorithms; ii) since the flash memory can be in system programmed it is possible to add or change algorithms or programmes to the firmware permanently.

It is also allowed to keep, in a static way, parameters of an algorithm to later use.

A 32-bit TMS320C44 DSP from Texas Instruments, which can deliver up to 40 MIPS/80MFLOPS, is used in each APC channel. Its main function is to process data that has been acquired in the respective ADC circuit of the APC channel. It also controls the signals that are generated on the DAC circuit of each APC channel and the parameters of acquisition and signal generation such as the sampling rate of the ADC and the update rate of the DAC. A 32-bit 128 kword SRAM is assigned to the DSP for its own operation (data, program and stack purposes) and that is totally independent of the other APC channels (local bus of the DSP).

The acquisition circuit (Figure 10.3) of each APC channel is composed of a front end of electronics that conditions the signal to the appropriate voltage range of the ADC and protect it from out of range signals or spikes, an antialiasing filter, the 12-bit CLC952 ADC from Comlinear, and a 32kword FIFO memory. The total independent sampling rate of the acquisition is generated by a software programmable PLL that is controlled by the DSP and a PLD MACH211SP from Vantis. The digitised data coming from the ADC is kept in the FIFO memory and can be red by the DSP word by word or using one of the internal DMAs channels of the DSP.

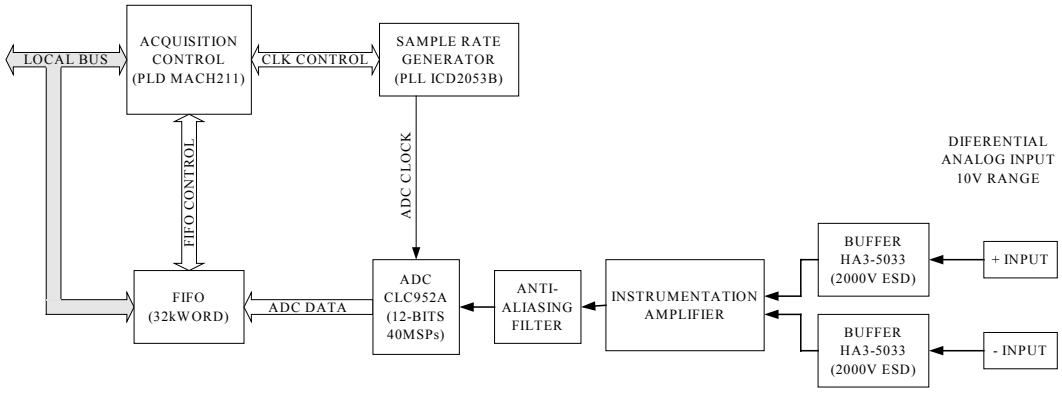

Figure 10.3 – Data acquisition architecture

The control and waveform generator circuit of each APC channel (Figure 10.4) incorporates a 32kword FIFO memory, a 14-bit HI5741 DAC and an output buffer HA3-5033 that can drive loads of 50 Ohms, both from Harris Semiconductor. The update rate of the DAC, as the sampling rate of the acquisition circuit, is also total independent and generated by a software programmable PLL that is controlled by the DSP and the PLD that control the local bus of each DSP. The DSP writes data only in the FIFO memory, and the PLD control all the remaining signals needed in order to output the control waveform. The PLD can be configured by the DSP in such a mode that enables the DAC circuit to generate periodic signals with up to 32k points without the intervention of the DSP.

The APC channels 1 and 3 have inputs to implement external hardware multiplying in the DAC circuit.

In order to avoid noise and cross talk between acquisition and control circuits of all APC channels, special attention was given to the design of board layout as well as in the isolation of power sources of the analog parts of differents circuits.

The interface of the module to the VME bus is made with a CY7C960A VME interface controller (VIC) chip and four CY7C964A VME bus driver chips, both from Cypress Semiconductor, and a high density PLD M5-256/120 from Vantis. Those from Cypress Semiconductor where specially designed to make the VME bus interface for any kind of VME transactions very simple to implement. In this slave module the transactions are A32/D16, the interrupt line 2 is used to interrupt the VME bus HOST and the address initialisation is compliant with the Auto Slot ID utility of the VME64 specification may be plug and play.

The VIC has a built-in DRAM refresh controller, which is used to control and refresh up to 4 Mwords of 16-bit of DRAM. This DRAM is shared, and can be accessed by the VME bus HOST and all the DSPs. For the VME bus it is in the A32 VME bus address space, for the DSPs it is in the address space of their global bus.

In this DSPs global bus address space there also: two FIFO memories that are used to send and receive commands between the VME bus HOST and the DSPs; the FLASH memory that contains the operative system of the DSPs; an optical digital input; an optical digital output and all the devices that belong to the EVENT bus interface.

In the M5-256/120 PLD is implemented all the decoding logic that is needed to decode all the devices that are in the address space of the global bus of the DSPs, as well as the arbiter that gives the control of the DSPs global bus to each DSP and VME bus HOST.

Each DSP communicate each other through three of the four high-speed parallel communication ports that they have. The DSPs of APC channels 0 and 1 can also communicate with a DSP in another module in the same crate (Figure 10.5).

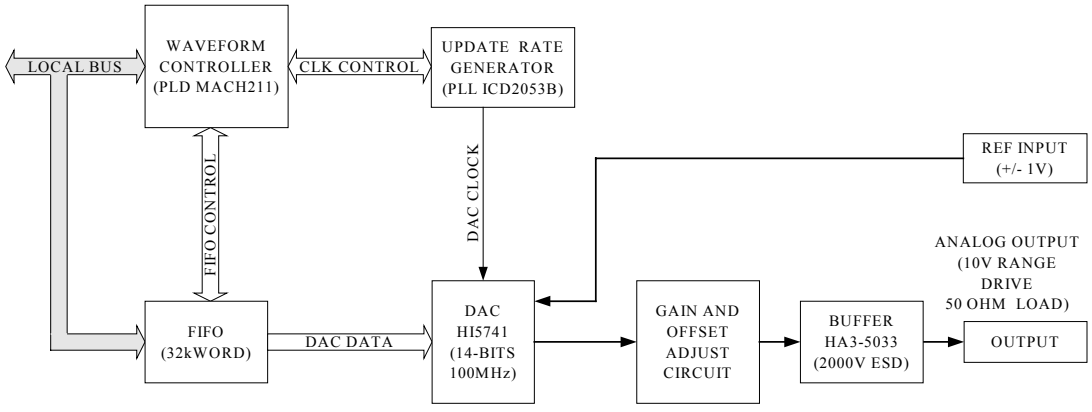

Figure 10.4 – Control and waveform generator architecture

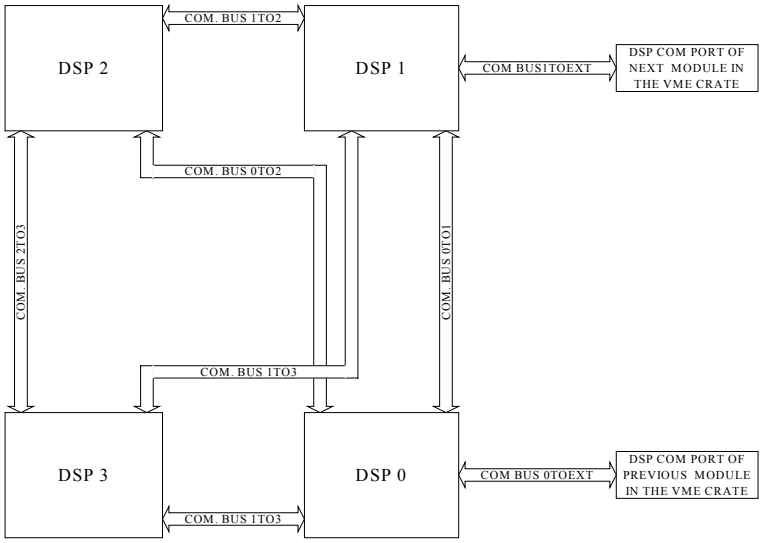

Figure 10.5 – DSP inter-communications buses structure

There are no configuration jumpers on the module. All the hardware configurations or the software that exists in the board can be in system programmed by JTAG interface or under software control.

The software of the module is organised in three parts: (i) the Operative System of each DSP; (ii) the application that each DSP runs; and (iii) the drivers that the VME bus HOST application use to communicate with the module.

The Operative System (OS) of each DSP consists in the library functions that give access to all the resources of the module and the kernel that manages the communications between DSPs and the VME bus HOST. This communication consists in commands with parameters that are sent and received through FIFO memories.

The application that each DSP ran may be downloaded from the HOST, or it can be programmed in the FLASH memory, and consists in a program that calls the OS library functions to access the module resources to get data and processing it in real-time or to generate control signals as needed. Normally, these programs are digital signal processing algorithms such as FFT, IIR, FIR, Convolution, Correlation, cross-correlation, etc.

More complex programs involving more than one DSP (parallel processing) may be designed when real-time calculations need to be done in less time. Two ways of parallel processing can be designed: (i) more than one DSP process differents slices of data of the same signal with the same algorithm at the same time; (ii) more than one DSP process the same data of the same signal with differents algorithms at the same time.

When real-time power processing needs to be increased, a signal that is acquired in a APC channel may be distributed to the other DSPs in the same module or in a different modules in the same VME crate, creating this way, a chain of DSPs to real-time parallel processing.

The software drivers that the VME bus HOST application use to communicate with the module were designed for OS9 operative system, and for Windows 98/NT operative system that runs in embedded PCs VME modules.

10.4. DEVELOPMENT OF PCI INSTRUMENTATION FOR CONTROL AND DATA ACQUISITION

This project aims the development of a set of transient recorder and waveform generator modules that can fulfil the typical requirements on control and data acquisition of a fusion experiment.

The following main activities were carried out:

- Purchase of development tools for PCI and Compact PCI;
- Study of the PCI rules and of the requirements of the dynamic memory;
- Beginning of the conceptual design of a PCI transient recorder module, with 8 channels, 12

bits resolution, 3 MSPS maximum sampling rate and 64 Mbytes memory per channel.

10.5. VARIATIONAL APPROACH TO THE EXTRACTION OF QUADRATURES FROM BROADBAND REFLECTOMETRY SIGNALS

Reflectometry diagnostics are successful tools for the measurement of the electron density profile in fusion devices. They are based on the radar principle: a probing wave is injected into the plasma and propagates until it reaches a cutoff layer where reflection occurs. At the reflection point, the electron density is a well-known function of the injected wave frequency, which is varied to allow a given range of density values to be scanned. Naturally, in order to obtain the density profile, the position of the reflection point, which can be inferred from the time delay of the reflected wave, must also be determined. In fusion experiments such time delays are very small, and pulsed radar techniques adequate to measure them directly, currently under development, require yet further experimentation. In broadband reflectometry, time delays are obtained indirectly, from the phase difference between the reflected wave and the probing wave. The dependable retrieval of this phase difference is, therefore, of the utmost importance to the correct functioning of a broadband reflectometer.

Since reflectometry diagnostics produce real-valued signals, a necessary and fundamental first step toward the measurement of the above-mentioned phase difference consists in defining the concepts of amplitude and phase to be associated with such signals, which amounts to the construction of a complex signal, with suitable amplitude and phase, by adding an appropriate imaginary part to the real-valued signal. Now, a real-valued reflectometry signal can be expressed in terms of its in-phase and quadrature components, briefly referred to as the standard quadratures of the signal, which are to be retrieved, from the signal, by a so-called mixing procedure. Amplitude and phase are readily derived from the quadratures, thereby leading to the quadrature (or exponential) signal as the natural complex form to choose.

Recently, arguments have been advanced in favor of the analytic signal as a means to retrieve the phase from broadband reflectometry signals. Using the analytic signal is actually equivalent to the less disputable decomposition in quadratures, whenever the latter can be appropriately employed, which is the case when quadratures are suitably band-limited. However, such a spectral requirement on quadratures cannot be verified by an inspection of the real-valued signals. Therefore, in principle, signals may exist that will not lead to band-limited quadratures, and for which devices based on the standard quadrature model will not be effective. Actually, this is an academic question since the quadrature decomposition is constantly applied to all sorts of band-limited signals, with success. Nevertheless, while being practically equivalent to the standard quadrature model, it can be said that the scope of the analytic signal is, from the point of view of its theoretical derivation, more general than that of the standard quadrature model. In fact, the analytic signal can be independently introduced, departing from a few general, mild, and indispensable conditions, which indicates that it will retain physical significance for a large number of signals. The use of the analytic signal to define amplitude and phase of real-valued signals is thus strongly supported by both theoretical and practical arguments.

Now, a variational method exists to extract in-phase and quadrature components from real-valued signals, which also provides, as a by-product, the carrier frequency. In this method, for each possible positive value of the carrier frequency, a functional measure for the joint variation of the in-phase and quadrature components is minimized, using a standard Euler–Lagrange variational technique, and the outcome is subsequently swept in the carrier frequency to look for its minimum value. Through this minimization procedure, the variational approach retrieves quadratures that are as slow as possible. Therefore, a priori, it constitutes a natural means to define the quadratures of signals with slowly varying amplitude and frequency. There has been some discussion on the subject of whether, or not, the variational method provides better results than the analytic signal. In the case of narrowband signals, it has been shown that they provide approximately the same amplitude and phase. However, they clearly lead to distinct results in the case of non-narrowband signals, and theoretical arguments alone have been considered insufficient to make a final judgment on the value of the variational approach. In this work, the variational method is applied to the problem of phase extraction from broadband reflectometry signals. A comparison with the analytic signal is also performed, thereby

contributing to the assessment of both approaches. It is argued that, in practice, the variational approach yields similar results to the analytic signal, thus constituting a natural method to extract quadratures from the reflectometry signals, with the advantage over the standard quadrature method of providing the carrier frequency in an intuitive way.

The results of applying the variational method to a set of four reflectometry signals, $s(n)$, with n varying from 1 to $N=1024$ samples, which are associated with four microwave bands, are shown in Figure 10.6, where are depicted the normalized frequency θ_c^V corresponding to the calculated variational carrier frequency, the variational instantaneous frequency $\theta_i^V(n)$, the analytic signal $\theta_i^{AS}(n)$, the relative error $\varepsilon_V(n)$ with respect to the instantaneous frequency calculated via the analytic signal,

$$\varepsilon_V(n)=\frac{\left|\theta_i^V(n)-\theta_i^{AS}(n)\right|}{\left|\theta_i^{AS}(n)\right|}, \tag{10.1}$$

and the frequency ratio $\rho(n)=\left|\theta_i^V(n)/\theta_c^V\right|$. As can be seen in the last row, none of the four signals can be considered as strictly narrowband, which is particularly evident in the last channel. Still, the results are only slightly different from those obtained with the analytic signal. The error in estimating the instantaneous frequency is typically around 3% in the first three bands, and 6% in the last one. Obviously, the less the signals can be considered narrowband, that is, the larger the $\rho(n)$, the greater the error $\varepsilon_V(n)$. The global error estimates

$$E=\frac{\sum_{n=1}^{N}\left|h(n)-r(n)\right|}{\sum_{n=1}^{N}\left[s(n)^2+r(n)^2\right]}, \tag{10.2}$$

where $h(n)$ and $r(n)$ are the imaginary parts of the analytic signal and variational quadrature signals respectively, measure the difference between the variational quadrature signal and the analytic signal. As expected, they are 1.72%, 0.71%, 0.47%, and 2.30%, respectively, for the four bands, corresponding clearly to small values.

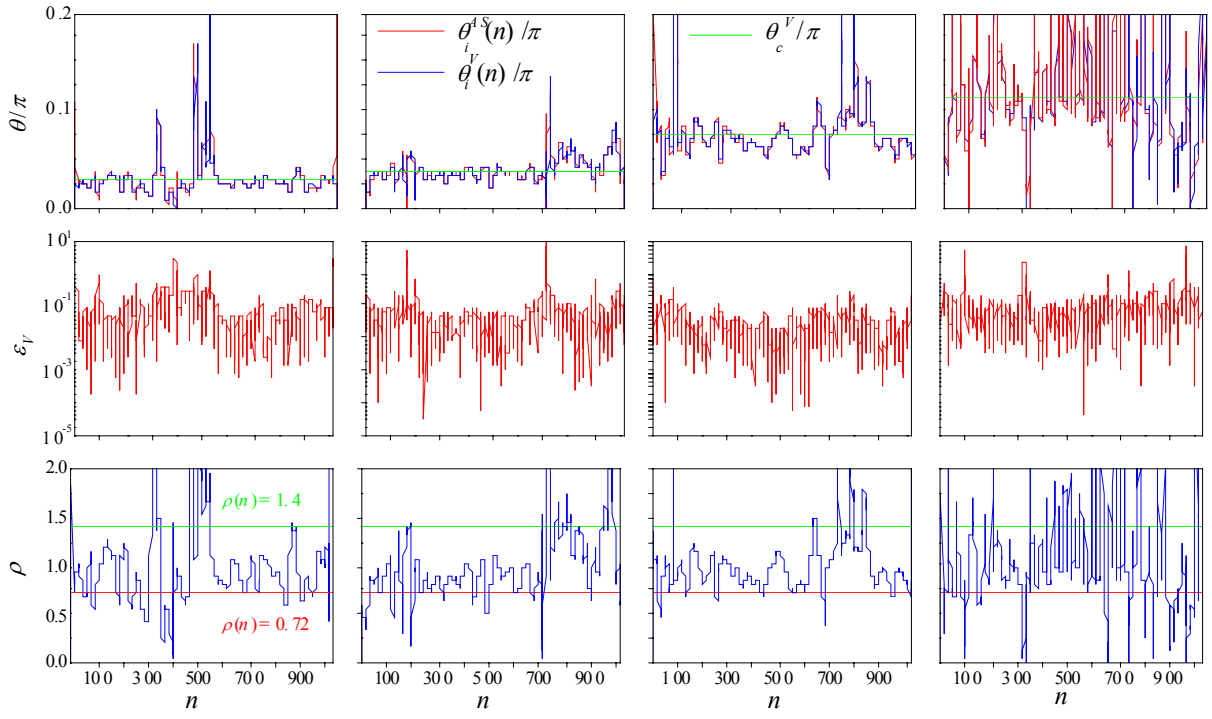

Figure 10.6 - Carrier frequencies, instantaneous frequencies, and relative errors for typical data from four O-mode reflectometry channels calculated using the analytic signal and the variational method.

In conclusion, a variational approach has been studied and applied to broadband reflectometry signals. For signals that are not narrowband the difference between both approaches can be substantial. In such cases, the variational approach is in contradiction with the functioning of widely used devices, based on the assumption of strictly band-limited quadratures, hence on the analytic-signal model. So, the variational approach to the extraction of the amplitude and phase of real-valued signals, which assumes only that quadratures are slowly time-varying, does not appear quite convincing when it disagrees with the analytic signal. Now, as far as reflectometry signals are concerned, it seems that, a priori and given its insightful derivation, the variational method is suited to model such signals. However, considering the solid arguments in favor of the analytic signal, it is important to assess if eventual differences between both approaches might turn the applicability of the variational method to reflectometry questionable. Actually, as shown in the present work, the variational method gives only slightly different results from the analytic signal, such a difference being perfectly acceptable. Since, in general, the obtained instantaneous-frequency estimates are to be smoothed in order to yield an average density profile, that difference becomes even more negligible. Moreover, even when using reflectometry diagnostics to study density fluctuations, as well as other phenomena requiring high resolution in the instantaneous phase derivative, it will be difficult to notice significant differences between the results obtained by the variational approach and those obtained with the analytic signal. Therefore, the variational method is an effective means to retrieve the phase from reflectometry signals, the intuitiveness behind its rationale constituting a conceptual advantage over the standard quadrature approach.