10. OTHER ACTIVITIES ON CONTROL, DATA ACQUISITION AND SIGNAL PROCESSING

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10.1. INTRODUCTION

This Project had two main research lines in 2002, concerning the development of:

- A fast, galvanic isolated, PCI data acquisition module;
- PCI time digitizers and transient recorders for the Neutron Diagnostics of the JET Enhancements Programme.

10.2. FAST, GALVANIC ISOLATED, PCI DATA ACQUISITION MODULE

10.2.1. Main activities

The following main activities were carried out:

- Conceptual design of the module;
- Elaboration of a proposal regarding the use of this module on the JET fast magnetics KC1F diagnostic;
- Discussion of this proposal with the EFDA Culham Close Support Unit;
- Beginning of the development of the circuit schematic.

10.2.2. Module description

The low-voltage signals generated in the KCF1 diagnostics are superimposed to a high common mode voltage. To measure these signals, differential amplifiers with high common mode rejection ratio (CMRR) are commonly used to separate the desired signal from the common mode voltage. In some cases the common mode voltage is too high to use standard differential amplifiers and a galvanic isolated amplifier should be used. This kind of amplifier can separate very high common mode voltages, normally in the kV range, from the signal to be measured.

The PCI-TR-256 module was designed as a multi-channel transient recorder which has 8 galvanic isolated inputs up to 1 kV RMS. The module has enough onboard memory to digitize up to 256 MSamples at a frequency of 2 MHz simultaneously on all channels with a resolution of 14-bit. It includes real-time digital signal processing functions that allow the digital down sampling of the signals and also to readout raw and filtered data in real-time.

The module was designed for low cost in a full-length PCI format and can be readily modified to have 8 non-isolated differential channels, by taking off the galvanic isolation components and thereby reducing the total cost of the board.

The PCI-TR-256 module architecture may be divided in four main blocks, which are:

(i) An analog block which includes the Analog to Digital Converters (ADC), a data serializer, the galvanic isolation and DC-DC power supplies.

(ii) A Field Programmable Gate Array (FPGA) to implement de-serialization, synchronism, memory buffers and Digital Signal Processor (DSP) interface.

(iii) The timing logic block which provides distribution of timing signals inside the module and to the other boards.

(iv) A DSP from TI (TMS320C6415) which includes a standard Peripheral Computer Interface (PCI) interface and a Synchronous Dynamic Random Access Memory (SDRAM) controller which addresses up to 512 MB SDRAM Dual Inline Module (DIMM).

Figure 10.1 shows the architecture of the PCI-TR-256 module, where the data path between the four blocks is depicted.

10.3. TIME DIGITIZERS AND TRANSIENT RECORDERS FOR THE NEUTRON DIAGNOSTICS ENHANCEMENTS

10.3.1. Main activities

The following main activities were performed:

- Conceptual design of a PCI time digitizer module and a PCI transient recorder module taking into account the requirements of the neutron diagnostics of the JET Enhancement Programme;
- Elaboration of a proposal aiming at the use of these modules on the JET diagnostics;
- Discussion of the proposal with the Project Leader and the EFDA Culham Close Support Unit.

10.3.2. Time digitizers

The time-of-flight neutron spectrometer (TOFOR) has of two groups of scintillator detectors which provide start and stop signals. The neutron flight times will be extracted from the time information of these signals. For every event originated in a detector, the time information

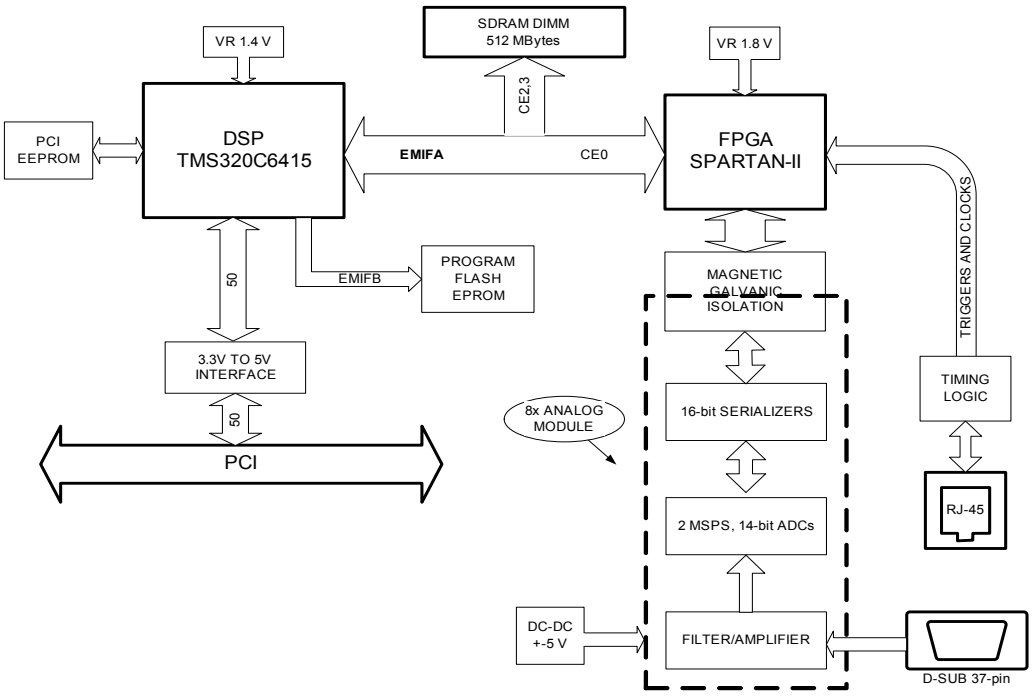

Figure 10.1 – The PCI-TR-256 module architecture

will be digitized and stored by a Time to Digital Converter (TDC).

Most of the existing TDC designs are based on the CMOS integrated circuit technology characterized by a time jitter in the order of the hundredths of picoseconds, thereby limiting the precision of the TDCs to a higher value. Existing LVPECL, based Gigabit Communications devices, can be used forr the design of an innovative TDC with a resolution equal or better than 500 ps and a time jitter of tenths of picoseconds. Due to the improved performance, the design approach is based on this technology as shown in Figure 10.2. This approach allows grouping channels in order to improve the time resolution (e.g. a resolution of 50 ps can be attained using eight 0.4 ns input channels) which is desirable in some cases.

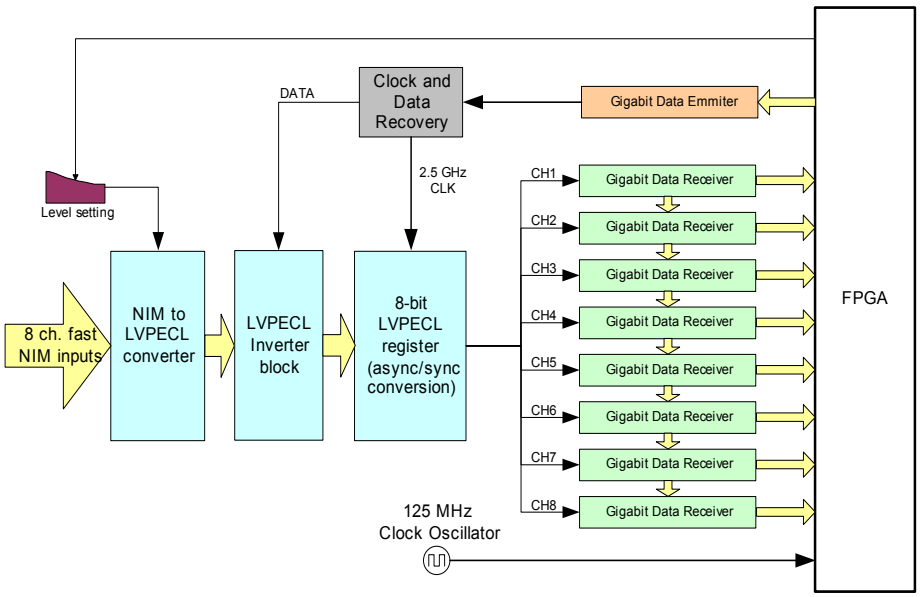

Figure 10.2 – The 2.5 GHz PECL time to digital converter

10.3.3. Transient recorders

The magnetic protion recoil neutron spectrometer (MPRu) includes 32 Phoswich laminated scintillators. Each scintillator detector is read out by two photomultiplier tubes. The shape of the pulses from the PM tube is digitized and stored for later analysis in a fast transient recorder.

The design of a low cost, four channels, fast (200 MSPS) PCI transient recorder, with a large amount of memory (64 MS/ch), was accomplished in order to cover the requirements of this diagnostic.

Figure 10.3 details the continuous acquisition design approach (for one input) which permitted to cover most of the requirements issues. A Field Programmable Gate Array (FPGA) contains a circular input buffer and a pipeline buffer to store the digitized pulses in each independent ADC channel. This approach requires no dead time between pulses and allows choosing any combination of pre-trigger and post-trigger depth up to a sum of 256 samples, storing pulse data at the maximum speed of 200 MSPS.

Similarly as in the PCI-TR-256, the digitized pulses in the FPGA pipeline are transferred to the DSP fast internal memory and afterwards stored it in the main memory. The stored data can then be accessed through the PCI interface by the host computer.

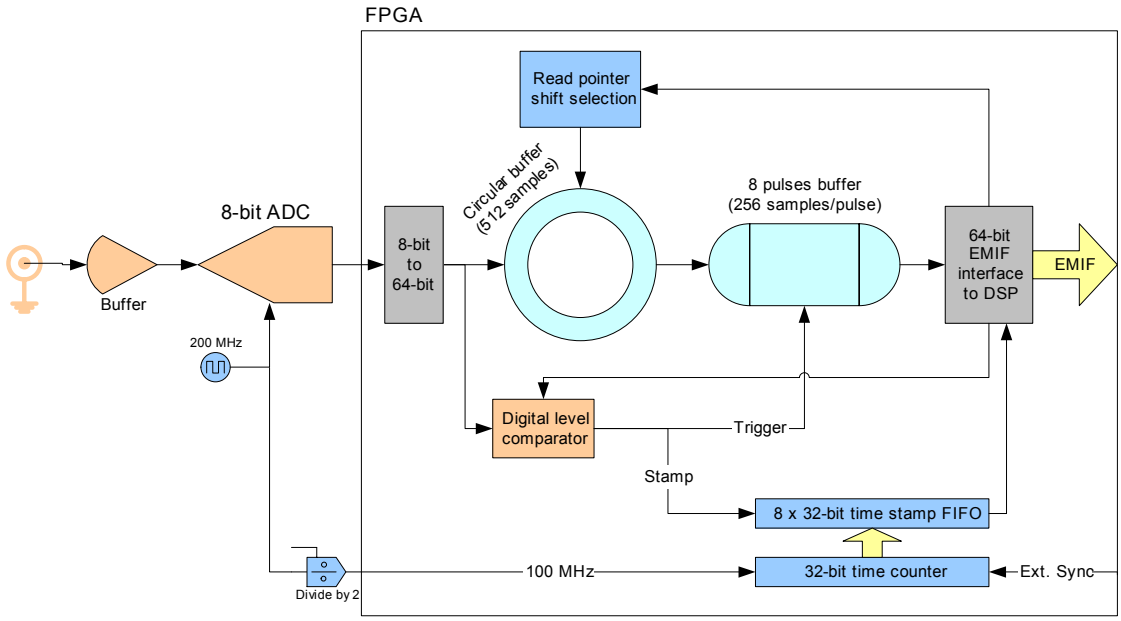

Figure 10.3 - Control and data flow through the FPGA for one ADC channel