### 9. OTHER ACTIVITIES ON CONTROL DATA ACQUISITION AND SIGNAL PROCESSING

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### 9.1. INTRODUCTION

This project concerns the activities on control, data acquisition and signal processing that are not included in the previous projects. The 2005 work programme has been essentially focused in four main working lines:

- Development of a data acquisition system for the ETE tokamak;
- Participation in the CASTOR programme on data acquisition;
- Development of a low-cost, fully integrated, eventdriven real-time control and data acquisition system for fusion experiments;
- Development of a time digitizer and transient recorder hybrid module for the enhanced neutron diagnostics data acquisition system

Concerning the development of a complete data acquisition system for  $ETE^{1}$ , the system architecture has been designed, including 64 transient recorder channels, a timing module and a CORBA based control and signal visualization software. Eight transient recorder modules were assembled and tested in 2005.

The participation in the CASTOR<sup>2</sup> programme on data acquisition has included the development of a complete data acquisition system, including 72 transient recorder channels as well as a CORBA based control and signal visualization software. Nine transient recorder modules, each one providing eight galvanic isolated channels, have been designed, assembled, mounted on an industry standard ATAC rack and functionally tested.

The overall architecture of *a low-cost*, *fully integrated*, *event-driven real-time control and data acquisition system for fusion experiments* was planned.

Regarding the *time digitizer and transient recorder hybrid module for the enhanced neutron diagnostics data acquisition system*, the module architecture has been defined accordingly to the specificities of the diagnostics, the acquisition module has been designed and the adequate software, firmware and hardware platforms have been identified.

## 9.2. PCI TRANSIENT RECORDER MODULE WITH GALVANIC ISOLATION

This module (Figure 9.1) has eight differential acquisition channels, performing a sampling rate up to 2 MSPS with 14-bit resolution. Each channel is galvanicly isolated by means of a magneto-coupler device. The input dynamic range is settable to  $\pm 10V$ ,  $\pm 5V$ ,  $\pm 2.5V$ ,  $\pm 2V$ ,  $\pm 0.5V$ . Data from each channel is serialized by a local PLD.

The main component of this module is its TMS320C6415<sup>TM</sup> DSP, which interfaces with the PCI bus, handles data processing tasks, and performs control of onboard memory. The use of state-of-the-art Field Programmable Gate Array (FPGA). (Xilinx Spartan 3 series) allows the implementation of data de-serialization, data synchronism and buffering and even the integration of digital data filters. A maximum storage of 512 MWords is available, in SDRAMM DIMM format.

The module has both internal and external clock and trigger capabilities, configurable to either TTL or RS-485 standards. A dedicated bus permits the synchronization of a maximum of 8 units within the same host.

### 9.3. LOW-COST, FULLY INTEGRATED, EVENT-DRIVEN REAL-TIME CONTROL AND DATA ACQUISITION SYSTEM

The overall architecture of this system (Figure 9.2) was designed based on the PCI Express, Advanced Switching Interconnect (ASI) and Advanced Telecommunications Computer Architecture (ATCA) standards, to be scalable both in performance and number of input signals, to permit the transport of signals and events in real-time (<1  $\mu$ s), to have all nodes synchronized over the gigabit data interconnections (clock, time, triggers), include Ethernet, ATM, PCI-X bridges and to provide automatic recognition of each node features through a XML description for easy integration on existing platforms.

Initially the following modules will be implemented: ATCA ix86-based controller; an (ii) (i) а digitizer/generator/processing card with 16 analogue input channels sampling at a rate up to 50 MSPS@12-bit, 4 analogue output channels, 8 digital IO channels and a state-of-the-art DSP and FPGA for real-time signal processing, and data flow control; (iii) a spectroscopy transient recorders with 4(2) channels sampling at a rate up to 200(400) MSPS@12-bit, 100(200) MSPS@14-bit and 1(2) GSPS@8-bit; and (iv) an ASI switch-fabric interconnection module and an ASI to ATM bridge.

<sup>&</sup>lt;sup>1</sup> ETE is a tokamak of the 'Laboratório Associado de Plasma do Instituto Nacional de Pesquisas Espaciais', de São José dos Campos, Brazil.

 $<sup>^2</sup>$  CASTOR is a tokamak of the Association Euratom/ IPP.CR (Institute of Plasma Physics), Prague.



Figure 9.1 – View of the TCA transient recorder module with galvanic isolation.



Figure 9.2 - Overall architecture of the system and of one node.

# 9.4. TIME DIGITIZER AND TRANSIENT RECORDER HYBRID MODULE

This module aims at: (i) implementing digital pulse processing (DPP) functions such as pulse height analysis (PHA) and pulse shape discrimination (PSD) for data reduction and real-time rough assessment of plasma parameters; (ii) fulfilling the requirements of the experiment diagnostics; (iii) having a high number of channels per board and consequently decreasing the cost per channel; and (iv) having an architecture designed for upgradeability and scalability. The module was designed for the ATAC bus with eight 12-bit resolution ADCs, providing eight analogue channels at 200 MSPS or, using a pair of digitizing channels shifted in phase (180°), four channels at 400 MSPS. Circuitry for using four ADCs to provide one channel at 800 MSPS is also included.

The module contains two FPGAs, each controlling a memory bank of 1 GB and four acquisition channels and providing a gigabit communications interface, thereby reducing circuit complexity and cost by acting as a system-on-chip device, (Figure 9.3).



Figure 9.3 – Simplified module block diagram

Only raw data (array of sampled pulses) is stored in memory. A continuous stream of processed data is sent to the ATCA controller for further processing and subsequent use for monitoring and control.