UPGRADE OF A FPGA-BASED TIMING BOARD WITH HIGH ACCURACY AND ANALYSIS OF TIMING PERFORMANCE IN KSTAR TOKAMAK OPERATION

Mikyung Park, W.R.Lee, and H.K. Na

National Fusion Research Institute (NFRI), Gwahangno 113, Yuseong-gu, Daejeon 305-333, Rep. of Korea

Coresponding Author : mkpark@nfri.re.kr

The newest superconducting tokamak device, KSTAR, performed successively to achieve the experimental goal of 300KA, 3second plasma in 2009 after the accomplishment of the first plasma in 2008. The missions of a timing system in tokamak are essentially to synchronize plant systems and control systems in accordance to operation scenarios for plasma experiments, and to provide accurate time information to order actions and events occurred, and to stamp time in data acquired. For those purposes, the timing board had been developed with distinguishing features and has performed sufficiently during the last two KSTAR campaign. However, as the experimental goals of KSTAR are evolving, more diagnostics even with mega-sampling acquisition are installed and require higher timing accuracy. Moreover, to support longer pulse plasma experiment, more flexible and diverse configuration in synchronized operation is needed. Therefore, the timing board has been upgraded to aim to improve accuracy in timing and to reduce noise in multiple trigger/clock output ports due to crosstalk between them while retaining all features of the old board such as PMC foam-factor, FPGA-based, EPICS interface, 64-bit data frame, reference to GPS time, central & local timing functions in single board, and so on. The other improvement is to add functionality to support longer pulse experiments by expanding the number of multi-gating sections in timing configuration and increasing utilization of output ports. The key features of the upgrade timing board as follows; timing accuracy less than 100ns, timing resolution of 5ns, sampling clock frequency from 1Hz to 100MHz, 10 multi-gating sections and PCI/PCI-x supported. All those improvements can be achieved by eliminating all software contributions and by implementing every processing in a FPGA chip with more number of gates. In addition, a frequency of master clock is raised up to 200MHz and some modifications in a PCB design are done to increase immunity to noise.
This paper will mainly describe the development of high accurate timing board of KSTAR and its performance. Moreover, it will explain the basic analysis of timing error to effect on the sequential operation of tokamak and relation with the performance of plasma experiment after investigation during the 2010 campaign in KSTAR.

[1] M.K.Park et al., Fusion Engineering and Design, volume 81 , 2006, pp 1817 ~ 1821
[2] G.Raupp et al., “The Timing System for ASDEX Upgrade”, The 7th IAEA technical Meeting on Control, 2009